What is claimed is:

1. A machine-implemented method comprising:

sampling machine instructions being performed by a processor;

identifying instruction types of the sampled machine instructions; and

presenting a metric indicating utilization of the processor by identified instruction types.

2. The method of claim 1, wherein sampling the machine instructions comprises:

identifying machine instructions to be retired from the processor; and

storing information corresponding to the machine instructions to a shared memory region.

3. The method of claim 2, wherein identifying machine instructions to be retired from the processor comprises reading a reorder buffer in the processor.

4. The method of claim 2, wherein the shared memory region comprises physical memory, and identifying the instruction types comprises decoding the information stored in the shared memory region.

5. The method of claim 2, wherein presenting the metric comprises displaying a representation of real-time instruction mix utilization including an indication of a percent of the machine instructions that are optimized for the processor.

6. The method of claim 2, wherein sampling the machine instructions occurs in kernel-mode, identifying the instruction types occurs in user-mode, and presenting the metric occurs in user-mode.

7. The method of claim 1, further comprising selecting the instruction types to be identified from a set of available instruction categories based on received input.

8. The method of claim 1, further comprising logging to an output file the utilization of the processor by identified instruction types.

9. The method of claim 1, further comprising:

presenting a user interface capable of receiving adjustments to a sampling interval and a sampling rate; and

adjusting the sampling of machine instructions based on input received via the user interface.

10. The method of claim 1, further comprising displaying actual processor speed in real time as the speed varies.

11. An article comprising a machine-readable medium embodying information indicative of instructions that when performed by one or more machines result in operations comprising:

identifying instruction types of sampled machine instructions being performed by a processor; and

presenting a metric indicating utilization of the processor by identified instruction types.

12. The article of claim 11, wherein the machine instructions comprise instructions to be retired from the processor, and identifying the instruction types comprises decoding stored information corresponding to the machine instructions to be retired.

13. The article of claim 11, wherein presenting the metric comprises displaying a representation of real-time instruction mix utilization including an indication of a percent of the machine instructions that are optimized for the processor.

14. The article of claim 11, wherein the operations further comprise selecting the instruction types to be identified from a set of available instruction categories based on received input.

15. The article of claim 11, wherein the operations further comprise logging to an output file the utilization of the processor by identified instruction types.

16. The article of claim 11, wherein the operations further comprise:

presenting a user interface capable of receiving adjustments to a sampling interval and a sampling rate; and

adjusting the sampling of machine instructions based on input received via the user interface.

17. The article of claim 11, wherein the operations further comprise displaying actual processor speed in real time as the speed varies.

18. A system comprising:

a shared memory that receives information corresponding to a subset of machine instructions retired from a processor; and

an instruction mix monitor that identifies instruction types based on the information in the shared memory and presents a metric indicating utilization of the processor by identified instruction types.

19. The system of claim 18, wherein the shared memory comprises physical memory.

20. The system of claim 18, wherein the instruction mix monitor comprises a display presentation that shows a representation of real-time instruction mix utilization, including an indication of a percent of the machine instructions that are optimized for the processor.

21. The system of claim 20, wherein the instruction mix monitor further comprises an instruction categories selection interface.

22. The system of claim 20, wherein the instruction mix monitor further comprises an instruction logging control interface.

23. The system of claim 20, wherein the instruction mix monitor further comprises a sampling adjustment control interface.

24. The system of claim 20, wherein the instruction mix monitor further comprises a display presentation that shows actual processor speed in real time as the speed varies.

25. A system comprising:

means for monitoring instruction mix in a processor; and

means for displaying in real time the monitored instruction mix in the processor.

26. The system of claim 25, further comprising means for displaying processor frequency in real time.